



CMLDM7003  
CMLDM7003G\*  
CMLDM7003J

**SURFACE MOUNT PICOmini™  
DUAL N-CHANNEL  
ENHANCEMENT-MODE  
SILICON MOSFET**

**PICOmini™**



**SOT-563 CASE**

\* Device is **Halogen Free** by design

# Central™ Semiconductor Corp.

## DESCRIPTION:

These CENTRAL SEMICONDUCTOR devices are dual Enhancement-mode N-Channel Field Effect Transistors, manufactured by the N-Channel DMOS Process, designed for high speed pulsed amplifier and driver applications. The CMLDM7003 utilizes the USA pinout configuration, while the CMLDM7003J utilizes the Japanese pinout configuration. These devices offer low  $r_{DS(ON)}$  and ESD protection up to 2kV.

**MARKING CODES:** CMLDM7003: **C30**  
CMLDM7003G\*: **C3G**  
CMLDM7003J: **C3J**

## MAXIMUM RATINGS: ( $T_A=25^\circ\text{C}$ )

Drain-Source Voltage  
Drain-Gate Voltage  
Gate-Source Voltage  
Continuous Drain Current  
Maximum Pulsed Drain Current  
Power Dissipation (Note 1)  
Power Dissipation (Note 2)  
Power Dissipation (Note 3)  
Operating and Storage Junction Temperature  
Thermal Resistance

SYMBOL		UNITS
$V_{DS}$	50	V
$V_{DG}$	50	V
$V_{GS}$	12	V
$I_D$	280	mA
$I_{DM}$	1.5	A
$P_D$	350	mW
$P_D$	300	mW
$P_D$	150	mW
$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$
$\Theta_{JA}$	357	$^\circ\text{C/W}$

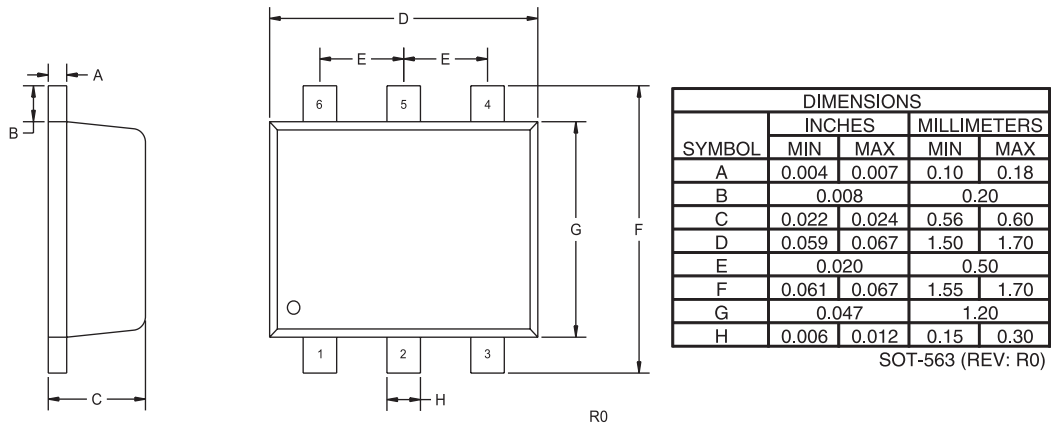
## ELECTRICAL CHARACTERISTICS PER TRANSISTOR: ( $T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{GSSF}, I_{GSSR}$	$V_{GS}=5.0\text{V}$			100	nA
$I_{GSSF}, I_{GSSR}$	$V_{GS}=10\text{V}$			2.0	$\mu\text{A}$
$I_{GSSF}, I_{GSSR}$	$V_{GS}=12\text{V}$			2.0	$\mu\text{A}$
$I_{DSS}$	$V_{DS}=50\text{V}, V_{GS}=0\text{V}$			50	nA
$BV_{DSS}$	$V_{GS}=0\text{V}, I_D=10\mu\text{A}$	50			V
$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.49		1.0	V
$V_{SD}$	$V_{GS}=0\text{V}, I_S=115\text{mA}$			1.4	V
$r_{DS(ON)}$	$V_{GS}=1.8\text{V}, I_D=50\text{mA}$		1.6	3.0	$\Omega$
$r_{DS(ON)}$	$V_{GS}=2.5\text{V}, I_D=50\text{mA}$		1.3	2.5	$\Omega$
$r_{DS(ON)}$	$V_{GS}=5.0\text{V}, I_D=50\text{mA}$		1.1	2.0	$\Omega$
$g_{FS}$	$V_{DS}=10\text{V}, I_D=200\text{mA}$	200			mS
$C_{rss}$	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			5.0	pF
$C_{iss}$	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			50	pF
$C_{oss}$	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$			25	pF

Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0 mm<sup>2</sup>  
(2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0 mm<sup>2</sup>  
(3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4 mm<sup>2</sup>

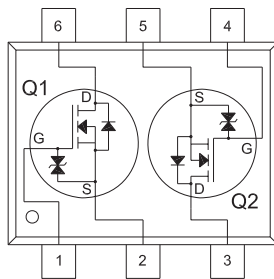
R5 (8-January 2009)

### SOT-563 CASE - MECHANICAL OUTLINE



### PIN CONFIGURATIONS

CMLDM7003 (USA Pinout)  
CMLDM7003G\*

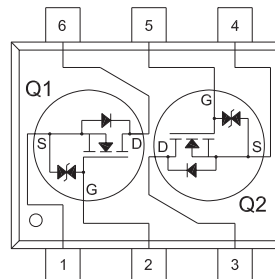


**LEAD CODE:**

- 1) GATE Q1
- 2) SOURCE Q1
- 3) DRAIN Q2
- 4) GATE Q2
- 5) SOURCE Q2
- 6) DRAIN Q1

**MARKING CODES:** CMLDM7003: C30  
CMLDM7003G\*: C3G

CMLDM7003J (Japanese Pinout)



**LEAD CODE:**

- 1) SOURCE Q1
- 2) GATE Q1
- 3) DRAIN Q2
- 4) SOURCE Q2
- 5) GATE Q2
- 6) DRAIN Q1

**MARKING CODE:** C3J

\* Device is **Halogen Free** by design